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PATENT
Docket No. SPLX.P0012

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 23, 2004.

Mari Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig

Serial No.: 09/737,245

Filing Date: 12/13/2000

For: METHOD AND APPARATUS FOR
USING CONNECTION GRAPHS WITH
POTENTIAL DIAGONAL EDGES TO
MODEL INTERCONNECT
TOPOLOGIES DURING PLACEMENT

Examiner: Thuan Do

Group Art Unit: 2825

**REQUEST FOR RECONSIDERATION OF PETITION UNDER 37 CFR § 1.137 (B)/(F)
AND WITHDRAWAL OF HOLDING OF ABANDONMENT UNDER 37 C.F.R. § 1.181**

Mail Stop Petition
Director of the US Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant hereby petitions the Director of the US Patent and Trademark Office to reconsider the petition under 37 CFR § 1.137 (b)/(f) and withdraw the holding of abandonment under 37 C.F.R. § 1.181 for the above-identified U.S. patent application.

On June 3, 2003, the Applicant submitted a petition under 37 CFR § 1.137 (b)/(f) to revive the above-mentioned application. On July 8, 2004, the Petition was dismissed on the

grounds that "the above-identified application was abandoned for not timely responding to the non-final Office action dated 12/4/2002". *See* copy of the Decision on the petition under 37 CFR § 1.137 (f).

The Applicant acknowledges that on March 4, 2003 the Applicant filed a Response to the Office Action. The Applicant received a return receipt postcard indicating that the PTO received the Response on March 10, 2003. *See* copy of the return receipt postcard. Therefore, the Applicant respectfully requests Director of the US Patent and Trademark Office to reconsider petition under 37 CFR § 1.137 (f) and to withdraw the holding of abandonment for the above-identified U.S. patent application.

In support of this petition, the Applicant encloses:

1. A copy of the Amendment (19 pages);
2. A copy of the Transmittal Letter for Response to an Office Action (2 pages);
3. A copy of the Credit Card Payment Form;
4. A copy of the Decision on the petition under 37 CFR § 1.137 (f) (2 pages); and
5. A copy of a return receipt postcard that accompanied the Amendment that the US PTO dated March 10, 2003 (1 page).

There is no fee associated with this petition as the Applicant timely responded to the Office Action and the application has been erroneously held abandoned. However, in the unlikely event that the Patent Office determines that additional fee is required, Applicant

authorizes the Assistant Commissioner to charge the cost of such fees to **Deposit Account**
No. 50-1128 referencing SPLX.P0012.

Respectfully submitted,

Dated: 7/23/2004

By: _____

Mari Adeli
Registration No. 39,585

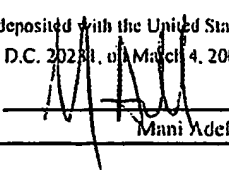
Stattler, Johansen & Adeli LLP
P.O. Box 51860
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PATENT
Docket No. SPLX.P0012

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Assistant Commissioner for Patents, Washington, D.C. 20231, on March 4, 2003.


Mami Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig

Serial No.: 09/737,245

Filing Date: 12/13/00

For: METHOD AND APPARATUS FOR
USING CONNECTION GRAPHS WITH
POTENTIAL DIAGONAL EDGES TO
MODEL INTERCONNECT
TOPOLOGIES DURING PLACEMENT

Examiner: Thuan Do

Group Art Unit: 2825

TRANSMITTAL LETTER FOR RESPONSE TO AN OFFICE ACTION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In complete response to the Office Action dated 12/4/02, attached please find:

1. An Amendment to the Office Action;
2. A Return Receipt Post Card.
3. A Credit Card Payment Form is attached.

The fee has been calculated as follows:

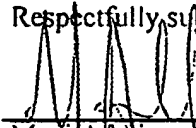
FOR	NUMBER	NUMBER OVER ALLOTMENT	RATE	CALCULATIONS
ADDED CLAIMS	9	9	x \$18.00	\$162.00
ADDED INDEPENDENT CLAIMS	1	1	x \$84.00	\$84.00
				TOTAL = \$246.00

The Assistant Commissioner is hereby authorized to charge any additional fees under 37 C.F.R. §§.1.16 and 1.17 that may be required by this transmittal and associated documents, or to credit any overpayment to Deposit Account No. 50-1128 referencing docket number: SPLX.P0012.

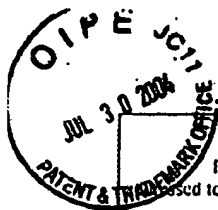
Dated: March 4, 2003

Respectfully submitted,

By:


Mani Adeli
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CERTIFICATE OF MAILING BY "FIRST CLASS MAIL."

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on Tuesday, March 04, 2003.

Muni Adeti

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application for:

Steven Teig et al.

Serial No.: 09/737,245

Filing Date: 12/13/00

For: METHOD AND APPARATUS FOR
USING CONNECTION GRAPHS WITH
POTENTIAL DIAGONAL EDGES TO MODEL
INTERCONNECT TOPOLOGIES DURING
PLACEMENT

Examiner: Thuan Do

Group Art Unit: 2825

AMENDMENT

Assistant Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

In response to the Office Action dated December 4, 2002, please amend the patent application as follows:

IN THE SPECIFICATION

Please replace the paragraph on page 11, lines 5-6 in the specification with the following amended paragraph.

--Figure 10, which is presented on two separate sheets labeled **Figure 10A** and **10B**, illustrates a process for generating a wirelength estimate according to a bounding-box method of the invention.--

Please replace the paragraph on page 11, lines 8-9 in the specification with the following

amended paragraph.

--**Figure 12**, which is presented on two separate sheets labeled **Figure 12A** and **12B**, illustrates a process for generating a wirelength estimate by constructing MST's that include horizontal, vertical, and 45° edges.--

Please replace the paragraph on page 11, lines 12-13 in the specification with the following amended paragraph.

--**Figure 14**, which is presented on two separate sheets labeled **Figure 14A** and **14B**, illustrates a process for generating a wirelength estimate by constructing Steiner trees with 45° diagonal edges.--

Please replace the paragraph on page 12, lines 3-4 in the specification with the following amended paragraph.

--**Figure 19**, which is presented on two separate sheets labeled **Figure 19A** and **19B**, illustrates a process that generates a congestion cost estimate, and partitions a set of nets, about a cut line.--

Please replace the paragraph on page 12, line 6 in the specification with the following amended paragraph.

--**Figure 23**, which is presented on two separate sheets labeled **Figure 23A** and **23B**, illustrates one example of a local optimization process.--

Please replace the paragraph on page 12, line 7 in the specification with the following amended paragraph.

--**Figure 24**, which is presented on two separate sheets labeled **Figure 24A** and **24B**, illustrates one example of a simulated annealing process.--

Please replace the paragraph on page 12, line 8 in the specification with the following amended paragraph.

--Figure 25, which is presented on two separate sheets labeled Figure 25A and 25B, illustrates one example of a KLFM process.--

IN THE CLAIMS

Please amend the claims in the application as follows:

43. (Amended) A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a net and a plurality of circuit elements, wherein the net represents interconnections between a set of circuit elements, the computer program comprising sets of instructions for:

constructing a connection graph that models the topology of interconnect lines for connecting the circuit elements of the net, wherein said connection graph having edges, each edge connecting two circuit elements of the net, wherein at least one of the edges is at least partially diagonal,

identifying a placement metric based on the connection graph.

44. (Amended) The computer readable medium of claim 43, wherein the set of instructions for identifying a placement metric comprises sets of instructions for:

calculating the length of the edges of the graph; and

combining the length calculations of the edges of the graph.

45. (Amended) The computer readable medium of claim 44, wherein the set of instructions for combining of said length calculations comprises a set of instructions for adding said measurements.

46. (Amended) The computer readable medium of claim 44, wherein to calculate the length of each edge that connects two circuit elements, the computer program further comprises sets of instructions for:

a) constructing a bounding box that encompasses the two circuit elements, said bounding box having a long side with a length L and a short side with a length S, said

diagonal edge forming an angle A with a side of the IC layout, wherein the two circuit elements are at two corners of the bounding box;

b) calculating the distance (D) between the two corners of the bounding box by using the equation $D = [L - \{S (\cos A / \sin A)\}] + S/\sin A$.

47. (Amended) The computer readable medium of claim 46, wherein the angle A corresponds to the angle of at least one type of interconnect-line in a wiring model used by the IC layout.

48. (Amended) The computer readable medium of claim 44, wherein the combined length calculation provides an estimate of interconnect-line length needed to connect the circuit elements of the net.

49. (Amended) The computer readable medium of claim 48, wherein said estimate is measured to obtain a placement cost of an initial placement configuration.

50. (Amended) The computer readable medium of claim 48, wherein the computer program further comprises sets of instructions for:

- a) modifying the position of at least one circuit elements of the net;
- b) after said modification,

constructing a second connection graph that models the topology of interconnect lines for connecting the circuit elements of the net, said second graph having a number of edges, each edge connecting two circuit elements, and

calculating the length of the edges of the second connection graph,

- c) to calculate the length of each edge that connects two circuit elements,

constructing a bounding box that encompasses the two circuit elements, said bounding box having a long side with a length L and a short side with a length S, wherein at least one type of interconnect-line in a wiring model used by the IC layout forms an angle A with a side of the IC layout;

calculating the length (D) of the edge by using the equation $D = [L - \{S (\cos A / \sin A)\}] + S/\sin A$.

d) combining the length calculations of the edges of the graph.

51. (Amended) The computer readable medium of claim 44, wherein the IC layout includes a plurality of nets, each net having a plurality of circuit elements, wherein the computer program further comprises sets of instructions for:

a) constructing, for each particular net, a connection graph that models the topology of interconnect lines for connecting the circuit elements of the particular net, said connection graphs having edges, wherein some of the edges are at least partially diagonal;

b) calculating the length of the edges of the graphs; and

c) combining the length calculations to obtain an estimate of the interconnect-line length needed for connecting the circuit elements of the nets.

52. (Amended) The computer readable medium of claim 43, wherein the diagonal edge forms a 45° angle with respect to a side of the IC layout.

53. (Amended) The computer readable medium of claim 43, wherein the diagonal edge forms a 120° angle with respect to a side of the IC layout.

54. (Amended) The computer readable medium of claim 43, wherein the circuit elements include pins of circuit modules.

55. (Amended) The computer readable medium of claim 43, wherein the circuit elements include circuit modules.

56. (Amended) The computer readable medium of claim 43, wherein the connection graph is a minimum spanning tree.

57. (Amended) The computer readable medium of claim 43, wherein the connection graph is a Steiner tree.

58. (Amended) A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the computer program uses a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the computer program comprising sets of instructions for:

a) defining, for each particular net, a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal,

b) calculating the length of the edges of the minimum spanning trees; and

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets.

59. (Amended) The computer readable medium of claim 58, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

60. (Amended) The computer readable medium of claim 58, wherein the computer program further comprises sets of instructions for:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) defining, for each net containing the moved circuit element, a new minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal,

c) calculating the length of the new minimum spanning trees to estimate the

change in the total interconnect-line length.

61. (Amended) A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the computer program uses a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the computer program comprising sets of instructions:

a) defining, for each particular net, a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said Steiner trees having edges, wherein at least one of the edges of at least one of the Steiner trees is at least partially diagonal;

b) calculating the length of the Steiner trees; and

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets.

62. (Amended) The computer readable medium of claim 61, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

63. (Amended) The computer readable medium of claim 61, wherein the computer program further comprises a set of instructions for defining a set of Steiner points for at least some of the nets.

64. (Amended) The computer readable medium of claim 61, wherein the computer program further comprises sets of instructions for:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) for each net containing the moved circuit element, defining a new Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the

particular net after the move, said new Steiner trees having edges, wherein at least one of the edges of at least one of the new Steiner trees is at least partially diagonal.

c) calculating the length of the new Steiner trees to estimate the change in the total interconnect-line length.

Please add the following claims 88-96.

--88. (New) A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a set of circuit elements, the computer program comprising sets of instructions for:

a) identifying a connection graph that models the topology of interconnect lines for connecting the set of circuit elements, wherein said connection graph has a plurality of edges, wherein at least some of the edges are neither parallel nor orthogonal to each other,

b) identifying a placement metric based on the connection graph.

89. (New) The computer readable medium of claim 88, wherein the set of instructions for identifying a placement metric comprises sets of instructions for calculating the length of the graph.

90. (New) The computer readable medium of claim 89, wherein the length provides an estimate of interconnect-line length needed to connect the circuit elements of the net.

91. (New) The computer readable medium of claim 90, wherein said placement metric estimate is identified to obtain a placement cost of an initial placement configuration.

92. (New) The computer readable medium of claim 90, wherein said placement metric estimate is identified to obtain a placement cost of a modified placement configuration.

93. (New) The computer readable medium of claim 88, wherein the edges that are neither parallel nor orthogonal forms a 45° angle with respect to each other.

94. (New) The computer readable medium of claim 88, wherein the edges that are

neither parallel nor orthogonal forms a 120° angle with respect to each other.

95. (New) The computer readable medium of claim 88, wherein the connection graph is a minimum spanning tree.

96. (New) The computer readable medium of claim 88, wherein the connection graph is a Steiner tree.--

REMARKS

In the Office Action dated December 4, 2002, the Examiner rejected claims 43-64 for statutory double patenting under 35 U.S.C. 101. The Examiner also rejected claims 43-45, 48, 49, 52-57 as being anticipated by USP 5,973,376 issued to Rostoker et al (Rostoker). The Examiner also objected to the specification for its description of Figures 10, 12, 14, 19, 23, 24, and 25, as this description did not mention that each of these drawings appears on two separate sheets.

In this Amendment, Applicants have amended the specification and claims 43-64. Applicants have also added new claims 88-96. Accordingly, claims 43-64 and 88-96 will be pending after entry of this Amendment.

I. Objection To The Description of the Drawings

In the Office Action, the Examiner objected to the description of Figures 10, 12, 14, 19, 23, 24, and 25, as this description did not mention that each of these drawings appears on two separate sheets. In this Amendment, applicants have amended the Brief Description of the drawings to state that each of these drawings appears on two separate sheets. For instance, the brief description of Figure 10 now states: "Figure 10, which is presented on two separate sheets labeled Figure 10A and 10B, ..." The descriptions of Figures 12, 14, 19, 23, 24, and 25 include similar annotations. Applicants respectfully request reconsideration and withdrawal of the objection to the description of the drawings.

II. Double Patenting Rejection

In the Office Action, the Examiner rejected claims 43-64 for statutory double patenting under 35 U.S.C. 101. The Examiner noted that filed claims 43-64 were identical to claims 43-64 in the parent application of the present application.

As filed, claims 43-64 recited methods for placing circuit modules in IC layouts. In this Amendment, Applicants have amended these claims to recite computer readable media that store computer programs for placing circuit modules in IC layouts. In this Amendment, Applicants have also added claims 88-96, which also recite computer readable media that store computer programs for placing circuit modules in IC layouts. Accordingly, Applicants respectfully submit that none of the pending claims claim the same subject matter as the method claims 43-64 of the parent application. Accordingly, Applicants respectfully request reconsideration and withdrawal of the statutory double patenting rejection.

III. Rejection of the Claims Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 43-45, 48, 49, 52-57 as being anticipated by Rostoker. Applicants respectfully submit that Rostoker does not anticipate any of these claims. These claims recite a computer readable medium that stores a computer program, which places circuit modules by constructing a connection graph with at least one edge that is at least partially diagonal. Rostoker does not disclose, teach, or even suggest a placer that places circuit modules by constructing a connection graph with at least one edge that is at least partially diagonal. To clarify this distinction further, Applicants have amended the body of independent claim 43, on which all the § 102 claims depend, to recite "identifying a placement metric based on the connection graph" with the at least one edge that is at least partially diagonal. In view of this amendment and the foregoing remarks, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection.

IV. New Claims 88-96

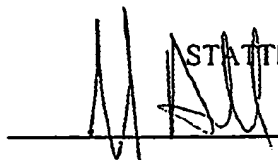
In this Amendment, Applicants have added new claims 88-96. Each of these claims recites a computer readable medium that stores a computer program, which places circuit modules in an IC layout. This computer program comprises sets of instructions for: (a) identifying a connection graph that models the topology of interconnect lines for connecting a set of circuit elements, where the connection graph has a plurality of edges and at least some of the edges are neither parallel nor orthogonal to each other, and (b) identifying a placement metric based on the connection graph. Applicants respectfully submit that all of the added new claims 88-96 are patentable over Rostoker.

CONCLUSION

In view of the foregoing, it is submitted that the currently pending claims, namely claims 43-64 and 88-96, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

Dated: 3/4/03



Mani Adeli
Reg. No. 39,585

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Palo Alto, CA 94303-0728
Phone: (650) 752-0990 ext.102
Fax: (650) 752-0995

AMENDED PARAGRAPHS FOR REPLACEMENT IN THE SPECIFICATION

The following pages provide the amended paragraphs for the specification with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

--Figure 10, which is presented on two separate sheets labeled Figure 10A and 10B,
illustrates a process for generating a wirelength estimate according to a bounding-box method of
the invention.--

Please replace the paragraph on page 11, lines 8-9 in the specification with the following
amended paragraph.

--Figure 12, which is presented on two separate sheets labeled Figure 12A and 12B,
illustrates a process for generating a wirelength estimate by constructing MST's that include
horizontal, vertical, and 45° edges.--

Please replace the paragraph on page 11, lines 12-13 in the specification with the
following amended paragraph.

--Figure 14, which is presented on two separate sheets labeled Figure 14A and 14B,
illustrates a process for generating a wirelength estimate by constructing Steiner trees with 45°
diagonal edges.--

Please replace the paragraph on page 12, lines 3-4 in the specification with the following
amended paragraph.

--Figure 19, which is presented on two separate sheets labeled Figure 19A and 19B,
illustrates a process that generates a congestion cost estimate, and partitions a set of nets, about a
cut line.--

Please replace the paragraph on page 12, line 6 in the specification with the following

amended paragraph.

--Figure 23, which is presented on two separate sheets labeled Figure 23A and 23B,
illustrates one example of a local optimization process.--

Please replace the paragraph on page 12, line 7 in the specification with the following
amended paragraph.

--Figure 24, which is presented on two separate sheets labeled Figure 24A and 24B,
illustrates one example of a simulated annealing process.--

Please replace the paragraph on page 12, line 8 in the specification with the following
amended paragraph.

--Figure 25, which is presented on two separate sheets labeled Figure 25A and 25B,
illustrates one example of a KLFM process.--

THE AMENDED CLAIMS

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

43. [For an electronic design automation application, a method of placing] A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a net and a plurality of circuit elements, wherein the net represents interconnections between a set of circuit elements, the [method comprising:] computer program comprising sets of instructions for:

constructing a connection graph that models the topology of interconnect lines for connecting the circuit elements of the net,

[said] wherein said connection graph having edges, each edge connecting two circuit elements of the net, wherein at least one of the edges is at least partially diagonal,

identifying a placement metric based on the connection graph.

44. The [method] computer readable medium of claim 43, wherein the set of instructions for identifying a placement metric comprises sets of instructions for: [further comprising]

calculating the length of the edges of the graph; and

combining the length calculations of the edges of the graph.

45. [The method] The computer readable medium of claim 44, wherein the set of instructions for combining of said length calculations comprises a set of instructions for adding said measurements.

46. [The method] The computer readable medium of claim 44, wherein to calculate the length of each edge that connects two circuit elements, the [method further comprises:]

computer program further comprises sets of instructions for:

a) constructing a bounding box that encompasses the two circuit elements, said bounding box having a long side with a length L and a short side with a length S, said diagonal edge forming an angle A with a side of the IC layout, wherein the two circuit elements are at two corners of the bounding box;

b) calculating the distance (D) between the two corners of the bounding box by using the equation $D = [L - \{S (\cos A / \sin A)\}] + S/\sin A$.

47. [The method] The computer readable medium of claim 46, wherein the angle A corresponds to the angle of at least one type of interconnect-line in a wiring model used by the IC layout.

48. [The method] The computer readable medium of claim 44, wherein the combined length calculation provides an estimate of interconnect-line length needed to connect the circuit elements of the net.

49. [The method] The computer readable medium of claim 48, wherein said estimate is measured to obtain a placement cost of an initial placement configuration.

50. [The method of claim 48 further comprising:] The computer readable medium of claim 48, wherein the computer program further comprises sets of instructions for:

a) modifying the position of at least one circuit elements of the net;

b) after said modification,

constructing a second connection graph that models the topology of interconnect lines for connecting the circuit elements of the net, said second graph having a number of edges, each edge connecting two circuit elements, and

calculating the length of the edges of the second connection graph,

c) to calculate the length of each edge that connects two circuit elements,

constructing a bounding box that encompasses the two circuit elements, said bounding box having a long side with a length L and a short side with a length S, wherein at least one type of interconnect-line in a wiring model used by the IC layout forms an angle A with a side of the IC layout;

calculating the length (D) of the edge by using the equation $D = [L - \{S (\cos A / \sin A)\}] + S / \sin A$.

d) combining the length calculations of the edges of the graph.

51. [The method] The computer readable medium of claim 44, wherein the IC layout includes a plurality of nets, each net having a plurality of circuit elements, [the method comprising:] wherein the computer program further comprises sets of instructions for:

a) constructing, for each particular net, [constructing] a connection graph that models the topology of interconnect lines for connecting the circuit elements of the particular net, said connection graphs having edges, wherein some of the edges are at least partially diagonal;

b) calculating the length of the edges of the graphs; and

c) combining the length calculations to obtain an estimate of the interconnect-line length needed for connecting the circuit elements of the nets.

52. [The method] The computer readable medium of claim 43, wherein the diagonal edge forms a 45° angle with respect to a side of the IC layout.

53. [The method] The computer readable medium of claim 43, wherein the diagonal edge forms a 120° angle with respect to a side of the IC layout.

54. [The method] The computer readable medium of claim 43, wherein the circuit elements include pins of circuit modules.

55. [The method] The computer readable medium of claim 43, wherein the circuit elements include circuit modules.

56. [The method] The computer readable medium of claim 43, wherein the connection graph is a minimum spanning tree.

57. [The method] The computer readable medium of claim 43, wherein the connection graph is a Steiner tree.

58. [For an electronic design automation application, a method of placing] A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the [EDA application includes] computer program uses a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the [method comprising:] computer program comprising sets of instructions for:

a) defining, for each particular net, [defining] a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal,

b) calculating the length of the edges of the minimum spanning trees; and

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets.

59. [The method] The computer readable medium of claim 58, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

60. [The method of claim 58 further comprising:] The computer readable medium of claim 58, wherein the computer program further comprises sets of instructions for:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) defining for each net containing the moved circuit element, [defining] a new minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal,

c) calculating the length of the new minimum spanning trees to estimate the change in the total interconnect-line length.

61. [For an electronic design automation application, a method of placing] A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the [EDA application includes] computer program uses a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the [method comprising:] computer program comprising sets of instructions:

a) defining for each particular net, [defining] a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said Steiner trees having edges, wherein at least one of the edges of at least one of the Steiner trees is at least partially diagonal;

b) calculating the length of the Steiner trees; and

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets.

62. [The method] The computer readable medium of claim 61, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

63. [The method of claim 61 further comprising] The computer readable medium of

claim 61, wherein the computer program further comprises a set of instructions for defining a set of Steiner points for at least some of the nets.

64. The [method] computer readable medium of claim 61, wherein the computer program further [comprising] comprises sets of instructions for:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) for each net containing the moved circuit element, defining a new Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said new Steiner trees having edges, wherein at least one of the edges of at least one of the new Steiner trees is at least partially diagonal,

c) calculating the length of the new Steiner trees to estimate the change in the total interconnect-line length.



PTO -2038 (02-2000) (Revised)

Approved for use through 1/31/2003. OMB 0651-0043

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Atty/Secty: MA

Filing Date: 12/13/00

Date Mailed: 3/4/2003

Atty Docket: SPLX.P0012

Applicant(s): Steven Teig

Title: Method and Apparatus for Using Connection Graphs with Potential Diagonal Edges to Model Interconnect Topologies During Placement

The following has been received by the U.S. PTO on the date stamped hereon:

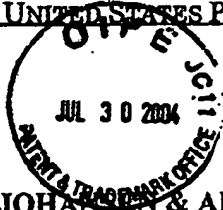
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OFFICE OF PETITIONS

In re Application of
Teig et al.
Application No. 09/737,245
Filed: December 13, 2000
Attorney Docket No. SPLX.P0012

ON PETITION

This is a decision on the petition under 37 CFR 1.137(f),¹ filed June 6, 2003, to revive the above-identified application.

The petition is **DISMISSED**.

The petition under 37 CFR 1.137(f) cannot be acted on due to the above-identified application already being abandoned for not timely responding to the non-final Office action mailed on December 4, 2002. No extensions of time under the provisions of 37 CFR 1.136(a) were obtained. Accordingly, this application became abandoned on March 5, 2003. Petitioner first needs to resolve that issue before the Office can act on the 1.137(f). Petitioner may wish to submit a petition under 37 CFR 1.137(b), which is enclosed for petitioner's convenience.

A grantable petition under 37 CFR 1.137(b) must be accompanied by:

- (1) the required reply,
- (2) the petition fee,
- (3) a statement that the entire delay in filing the required reply from the due date for the reply until the filing of a grantable petition pursuant to 37 CFR 1.137(b) was unintentional, and a terminal disclaimer and fee if the application was filed on or before June 8, 1995 or if the application is a design application.

Further correspondence with respect to this matter should be addressed as follows:

By mail: Mail Stop PETITION
Commissioner for Patents
Post Office Box 1450
Alexandria, VA 22313-1450

¹ 37 CFR 1.137(f) provides for revival of a nonprovisional application which became abandoned pursuant to the provisions of 35 U.S.C. § 122(b)(2)(B)(iii) for failure to timely notify the Office of the filing of an application in a foreign country or under a multinational treaty that requires publication of applications eighteen months after filing.

² In a nonprovisional application abandoned for failure to prosecute, the required reply may be met by the filing of a continuing application. In an application or patent, abandoned or lapsed for failure to pay the issue fee or any portion thereof, the required reply must be the payment of the issue fee or any outstanding balance thereof.

Effective December 1, 2003, the Office of Petitions can no longer receive hand-carried correspondence, or facsimile transmissions of correspondence. The centralized location for hand-carried correspondence is the existing Customer Window located at:

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The centralized facsimile number is (703) 872-9306.

Telephone inquiries should be directed to the undersigned at (703) 306-0482.



Liana Chase
Petitions Examiner
Office of Petitions
Office of the Deputy Commissioner
for Patent Examination Policy

Enclosure: PTO/SB/64 – Petition Under 37 CFR 1.137(b)

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